UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,527	10/03/2003	Roland A. Wood	H0001861 (1100.1214101)	1355

128 7590 01/04/2006

HONEYWELL INTERNATIONAL INC.
101 COLUMBIA ROAD
P O BOX 2245
MORRISTOWN, NJ 07962-2245

EXAMINER	
ZETTL, MARY E	

ART UNIT	PAPER NUMBER
2884	

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EJL

Office Action Summary	Application No.	Applicant(s)	
	10/678,527	WOOD ET AL.	
	Examiner	Art Unit	
	Mary Zettl	2884	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/16/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This action is in response to amendments and remarks filed on December 6, 2005. Claims 1-29 are currently pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 11, 12, 16, and 25-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki et al. (US 2005/0030399 A1).

Regarding claims 1, 25, 26 Suzuki et al. disclose a sensor comprising: a substrate (Figure 1, item 19 and Figure 3, item 39); an array of pixels situated on a single level on the substrate (Figure 1, item 11 and Figure 3, "pixel portion" and page 2, paragraph 36); and an electronics circuit situated on a single level horizontally proximate to the pixel (Figure 3, "peripheral circuit portion").

Regarding claims 11 and 12, Suzuki et al. disclose a thermal sensor comprising: a substrate (Figure 1, item 19 and Figure 3, item 39); an array of pixels situated on the substrate page (page 2; paragraph 36); and wherein: each

pixel is located on a single level (Figure 1, item 11 and Figure 3, "pixel portion") and is an infrared light detector (page 3, paragraph 44); an electronics circuit is associated with each pixel; and each electronic circuit is located on the single level with the pixel (Figure 3, "peripheral circuit portion").

Regarding claims 16 and 27-29, Suzuki et al. disclose a sensing means comprising: means for sensing infrared light (Abstract and page 3, paragraph 44); means for electronically processing signals related to infrared light sensed by the means for sensing infrared light (page 2, paragraph 35); and means for supporting on one level (or one surface or in a plane) the means for sensing infrared light and the means for electronically processing signals horizontally proximate to each other (page 2, paragraph 35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashio et al. (US 2001/0025926 A1).

Regarding claim 1, Mashio et al. teach a sensor comprising a substrate (Figure 2, item 1); a detecting portion situated on a single level on the substrate (Figure 2, item 2); and an electronics circuit situated on a single level (Figure 1,

item 7). Mashio et al. do not specify that the detecting portion is a pixel, however at the time the invention was made, one of ordinary skill would recognize that a pixel is a common means for detection.

Regarding claim 2, Mashio et al. teach the limitations set forth in claim 2, however do not disclose expressly a pixel wherein the fill factor is greater than 69 percent. However, in Figure 2, it appears that the detecting portion occupies an area greater than 69 percent and would thus indicate a fill factor greater than 69 percent although not explicitly stated.

Regarding claims 3-5, Mashio et al. teach the limitations set forth in claim 2, and further teach the pixel as an infrared light detector (Abstract), wherein the substrate has a pit proximate to the pixel (Figure 2, item 6) and the pixel has at least on via in the one level supporting the pixel (Figure 2).

Regarding claims 5-9, Mashio et al. further teach MOS circuitry (page 5, paragraph 79), which implies small area FET.

Regarding claim 10, Mashio does not disclose expressly a microbolometer, however the invention of Mashio has the features of a bolometer; a thermal sensor for detecting electromagnetic radiation (Abstract) including an absorber (paragraph 8). It would further be obvious to one of ordinary skill in the art that the sensor would be a microbolometer as microbolometers are less expensive to operate.

Regarding claim 23, Mashio et al. teach a sensor comprising: a substrate (Figure 2, item 1); a pixel (detecting portion) situated in a first plane relative to a

surface of the substrate (Figure 2, item 2); and an electronics circuit situated in the first plane (Figure 2, item 7).

Regarding claim 24, Mashio et al. teach a thermal sensor comprising: a substrate; and an array of pixels (detecting portions; Figure 2, item 2) situated on the substrate (Figure 2, item 1); and wherein: each pixel is located on a first surface; an electronic circuit is associated with each pixel; and each electronic circuit is located on the first surface proximate to the pixel (Figure 2, item 7).

Claims 13-15 and 17- 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US 2005/0030399 A1) in view of Mashio et al. (US 2001/0025926 A1).

Regarding claims 13 and 17, Suzuki et al. teach the limitations set forth in claims 12 and 16 respectively, however do not disclose expressly, each pixel suspended over a pit in the substrate. Mashio et al. teach the pixel as an infrared light detector (Abstract), wherein the substrate has a pit proximate to the pixel (Figure 2, item 6) and the pixel has at least on via in the one level supporting the pixel (Figure 2). At the time the invention was made it would be obvious to one of ordinary skill in the art to modify the invention of Suzuki et al. in view of Mashio et al. such that the substrate has a pit proximate to the pixel so as to provide thermal isolation.

Regarding claim 14, Suzuki et al. in view of Mashio et al. teach the limitations set forth in claim 13. Mashio et al. further teach MOS circuitry (page 5, paragraph 79), which implies small area FET.

Regarding claim 15, Suzuki et al. in view of Mashio et al. teach the limitations set forth in claim 14. Mashio does not disclose expressly a microbolometer, however the invention of Mashio has the features of a bolometer; a thermal sensor for detecting electromagnetic radiation (Abstract) including an absorber (paragraph 8). It would further be obvious to one of ordinary skill in the art that the sensor would be a microbolometer as microbolometers are less expensive to operate.

Regarding claim 18, Suzuki et al. in view of Mashio et al. teach the limitations set forth in claim 17. Mashio et al. further teach the means for electronically processing signals having an area that is a fraction of the area of the means for sensing infrared light (Figure 2).

Regarding claim 19, Suzuki et al. in view of Mashio et al. teach the limitations set forth in claim 18. Suzuki et al. further teach the means for sensing infrared light being an array of pixels (page 2, paragraph 36).

Regarding claims 20 and 21, Suzuki et al. in view of Mashio et al. teach the limitations set forth in claim 19. Mashio does not disclose expressly a microbolometer, however the invention of Mashio has the features of a bolometer; a thermal sensor for detecting electromagnetic radiation (Abstract) including an absorber (paragraph 8). It would further be obvious to one of ordinary skill in the art that the sensor would be a microbolometer as microbolometers are less expensive to operate. It would further be obvious to one of skill in the art that VO_x is an inherent component of a microbolometer. Mashio et al. further teach MOS circuitry (page 5, paragraph 79), which implies

small area FET. Suzuki et al. also teach CMOS circuitry (Abstract). Both teachings imply small area transistor circuitry.

Regarding claim 22, Suzuki et al. in view of Mashio et al. teach the limitations set forth in claim 21. Mashio et al. further teach wherein: the means for supporting on one level is a planar level substrate (Figure 2); and the thermal isolating opening is a pit in the substrate under each pixel of the array of pixels (Figure 2, item 6).

Response to Arguments

Applicant's arguments, see page 7, paragraph 2, filed December 6, 2005, with respect to claims 8 and 20 have been fully considered and are persuasive. The rejection of claims 8 and 20 has been withdrawn.

Applicant's arguments, see pages 7-9, filed December 6, 2005, with respect to the rejection(s) of claim(s) 1, 11, 12, 16, and 25-29 under 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Suzuki et al. (US 2005/0030399 A1).

Applicant's arguments, see pages 7-9, filed December 6, 2005, with respect to the rejection(s) of claim(s) 1-10, 23, and 24 under 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Mashio et al. (US 2001/0025926 A1).

Applicant's arguments, see pages 7-9, filed December 6, 2005, with respect to the rejection(s) of claim(s) 13-15 and 17- 19 under 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Suzuki et al. (US 2005/0030399 A1) in view of Mashio et al. (US 2001/0025926 A1).

Applicant's arguments, see pages 7-9, filed December 6, 2005, with respect to the rejection(s) of claim(s) 20-22 under 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Suzuki et al. (US 2005/0030399 A1) in view of Mashio et al. (US 2001/0025926 A1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Zettl whose telephone number is (571) 272-6007. The examiner can normally be reached on M-F 8am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MZ

DAVID PORTA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800